TITLE OF THE INVENTION

Semiconductor Device with Surge Protection Circuit

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor devices and more particularly to a semiconductor device having a surge protection circuit.

Description of the Background Art

There have been proposed various surge protection circuits for protecting, a motor vehicle, a motor, a fluorescent display and an audio device, for example, as well as an IC (Integrated Circuit) constituted of transistor devices for example, from an instantaneously increased current or voltage (surge). One of the proposed circuits, a surge protection circuit constituted of one diode and one npn transistor is known as a device which can be implemented with a simple configuration. A conventional surge protection circuit constituted of one diode and one npn transistor is configured as detailed below.

In the conventional surge protection circuit constituted of one diode and one npn transistor, the cathode of the diode has a first n^+ diffusion layer of high concentration formed at a main surface of a semiconductor substrate that is electrically isolated by a field oxide film. The first n^+ diffusion layer contacts a conductive layer formed on the semiconductor substrate and is thus connected electrically to a signal input terminal. The anode of the diode has a p-type diffusion layer and a p^+ diffusion layer formed in the p-type diffusion layer. The p^+ diffusion layer directly contacts the n^+ diffusion layer serving as the cathode.

Moreover, the collector of the npn transistor has the first n^+ diffusion layer, a buried n^+ diffusion layer and an n^- epitaxial layer formed in the semiconductor substrate. The base of the npn transistor has the p-type diffusion layer formed in the n^- epitaxial layer. The emitter of the npn transistor has a second n^+ diffusion layer formed in the p-type diffusion layer.

The first n^+ diffusion layer is included in the cathode region of the diode and included in the collector region of the npn transistor. Further,

the p-type diffusion layer is included in the anode region of the diode and in the base region of the npn transistor.

An operation of the above conventional surge protection circuit is now described. When a surge voltage is applied to the signal input terminal, the surge voltage is then applied to the first n^+ diffusion layer to increase a reverse voltage of the diode. This reverse voltage exceeding a certain level causes Zener breakdown of the diode and accordingly a current flows from the cathode to the anode of the diode. The p-type diffusion layer included in the anode region is also included in the base region of the npn transistor. Then, the current flows as a base current of the npn transistor. Accordingly, the npn transistor is turned on to discharge the charge of the surge applied to the signal input terminal from the emitter of the npn transistor.

Any surge protection circuits except for the above one are disclosed, for example, in Japanese Patent Laying-Open Nos. 5-206385 and 56-19657.

In the conventional surge protection circuit having the above-described configuration, the first n^+ diffusion layer is formed to have a high concentration in order to reduce contact resistance between the first n^+ diffusion layer serving as the cathode of the diode and the conductive layer mentioned above. Further, if a part of the anode region that contacts the first n^+ diffusion layer has a low concentration, electrons that are present in a depletion layer of the pn junction between the first n^+ diffusion layer and the anode (p-type diffusion layer) are trapped in the field oxide film adjacent to the first n^+ diffusion layer when breakdown of the diode occurs. Then, a problem arises that the depletion layer of the pn junction expands to increase the breakdown voltage of the diode. Therefore, it is required to form the p^+ diffusion layer of high concentration in a part, which contacts the first n^+ diffusion layer, of the p-type diffusion layer serving as the anode, in order to flow electrons from the first n^+ diffusion layer smoothly to the anode (p-type diffusion layer). In other words, both of the anode region and the cathode region constituting the pn junction where the Zener breakdown occurs should be formed with high concentration.

If, however, the anode region and the cathode region forming the pn

junction where Zener breakdown occurs are both formed with high concentration, the width of the depletion layer of the pn junction between the anode region and the cathode region is extremely small. A phenomenon (leakage of current) then occurs that is current flow in the surge protection circuit with any voltage lower than the breakdown voltage, resulting in a problem that the surge protection circuit does not operate normally.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device having a surge protection circuit without suffering from occurrence of current leakage and thus operating normally.

A semiconductor device according to the present invention includes a surge protection circuit electrically connected to a signal input terminal and having a diode and a transistor. The semiconductor device includes a semiconductor substrate having a main surface, a field oxide film formed at the main surface of the semiconductor substrate, and a conductive layer formed on the main surface of the semiconductor substrate and electrically connected to the signal input terminal. The diode has its cathode including a first cathode region and a second cathode region, the first cathode region is electrically connected to the conductive layer and formed at the main surface of the semiconductor substrate, and the second cathode region constitutes, together with an anode region of the diode, a pn junction where Zener breakdown occurs. The pn junction where the Zener breakdown occurs is distant from the field oxide film.

In the semiconductor device of the present invention, the first cathode region electrically connected to the conductive layer and the second cathode region constituting the pn junction where Zener breakdown occurs are separately formed. Therefore, the impurity concentration of the first cathode region can be increased to reduce contact resistance with the conductive layer. Moreover, the impurity concentrations of the anode region and the second cathode region can be reduced to prevent current leakage. Further, as the pn junction between the anode region and the second cathode region where Zener breakdown occurs is distant from the field oxide film, a problem that the breakdown voltage of the diode increases

can be solved. Here, the increase of the breakdown voltage is caused when electrons that are present in the depletion layer of the pn junction between the anode region and the cathode region are trapped in the field oxide film to expand the depletion layer of the pn junction. Accordingly, the semiconductor device having the surge protection circuit without suffering from current leakage and thus operating normally can be achieved.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a surge protection circuit in a first embodiment of the present invention.

Fig. 2 is a plan view schematically showing a configuration of a semiconductor device having the surge protection circuit in the first embodiment of the present invention.

Fig. 3 is a cross-sectional view along line III-III in Fig. 2.

Fig. 4A shows current-voltage characteristics of a semiconductor device having a conventional surge protection circuit, and Fig. 4B shows current-voltage characteristics of the semiconductor device having the surge protection circuit in the first embodiment of the present invention.

Fig. 5 is a plan view schematically showing a configuration of a semiconductor device having a surge protection circuit in a second embodiment of the present invention.

Fig. 6 is a cross-sectional view along line VI-VI in Fig. 5.

Fig. 7 is a cross-sectional view schematically showing a configuration of a semiconductor device having a surge protection circuit in a third embodiment of the present invention.

Fig. 8 is a plan view schematically showing a configuration of a semiconductor device having a surge protection circuit in a fourth embodiment of the present invention.

Fig. 9 is a cross-sectional view along line IX-IX in Fig. 8.

Fig. 10 is a plan view schematically showing a configuration of a

semiconductor device having a surge protection circuit in a fifth embodiment of the present invention.

Fig. 11 is a cross-sectional view along line XI-XI in Fig. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention are hereinafter described in connection with the drawings.

First Embodiment

Referring to Fig. 1, a surge protection circuit 31 includes a diode 22 and an npn transistor 23. The cathode of diode 22 and the collector of npn transistor 23 are electrically connected to a signal input terminal 21 and to a device portion 25. The anode of diode 22 and the base of npn transistor 23 are electrically connected to each other. The emitter of npn transistor 23 is electrically connected to a ground potential 24.

A configuration of a semiconductor device having the surge protection circuit in this embodiment is now described.

Referring to Figs. 2 and 3, a semiconductor device 51 has a p^- region 1 formed in a lower part of a semiconductor substrate 41 formed, for example, of silicon single crystal. On p^- region 1, an n^+ diffusion layer 2 is formed by implantation and diffusion. On this n^+ diffusion layer 2, an n^- epitaxial layer 4 is formed. On p^- region 1, a p^+ diffusion layer 3a and a p-type diffusion layer 6a are formed to enclose n^- epitaxial layer 4 and, a p^+ diffusion layer 9 is formed in p-type diffusion layer 6a. In n^+ diffusion layer 2 and n^- epitaxial layer 4, a p^+ diffusion layer 3b is formed by implantation and diffusion. Moreover, a field oxide film 7 is formed at the surface of semiconductor substrate 41 for electrically isolating regions of the semiconductor substrate from each other. Field oxide film 7 refers to a silicon oxide film formed by LOCOS (Local Oxidation of Silicon). P^+ diffusion layer 9, an n^+ diffusion layer 8a, an n^+ diffusion layer 8b and an n^+ diffusion layer 8c are thus electrically isolated from each other by field oxide film 7.

In this n^+ diffusion layer 2 and n^- epitaxial layer 4, diode 22 and npn transistor 23 constituting the surge protection circuit are formed. Diode 22 has an anode region and a cathode region while npn transistor 23 has an

emitter region, a base region and a collector region.

In diode 22, the anode region is constituted of a p-type diffusion layer 6b formed in an n-type diffusion layer 5. N-type diffusion layer 5 is formed in n^- epitaxial layer 4. The cathode region is constituted of n^+ diffusion layer 8c (first cathode region) formed in n^- epitaxial layer 4, n^- epitaxial layer 4, n-type diffusion layer 5, and n^+ diffusion layer 8b (second cathode region) formed in n-type diffusion layer 5 and p-type diffusion layer 6b.

In npn transistor 23, the collector region is constituted of n^+ diffusion layer 8c formed in n^- epitaxial layer 4, n^- epitaxial layer 4 and n^+ diffusion layer 2. The base region is constituted of p-type diffusion layer 6a formed in n^- epitaxial layer 4. The emitter region is constituted of n^+ diffusion layer 8a formed in p-type diffusion layer 6a.

In this embodiment, a pn junction where Zener breakdown occurs is formed of p-type diffusion layer 6b and n^+ diffusion layer 8b. N^+ diffusion layer 8b is formed to cover the upper surface of p-type diffusion layer 6b. With semiconductor substrate 41 viewed from the above (Fig. 2), n^+ diffusion layer 8b is seen to have its periphery electrically connected to n-type diffusion layer 5. Further, n-type diffusion layer 5 is formed to cover the side of p-type diffusion layer 6b. The cathode region constituted of n^+ diffusion layer 8b and n-type diffusion layer 5 is thus formed in the shape of a quadrangular prism and, in this quadrangular prism, p-type diffusion layer 6b serving as the anode region is formed. Accordingly, the pn junction (pn junction formed of p-type diffusion layer 6b and n^+ diffusion layer 8b) where Zener breakdown occurs is formed within the quadrangular prism, and is thus distant from field oxide film 7.

N-type diffusion layer 5 is formed by implantation of P (phosphorus) into n^- epitaxial layer 4 with an implantation dose, for example, of approximately 10^{12} ions/cm^2. P-type diffusion layers 6a and 6b are formed by implantation of B (boron) into n^- epitaxial layer 4 with an implantation dose, for example of approximately 10^{13} ions/cm^2. N^+ diffusion layers 8a-8c are formed by implantation of As (arsenic) to the surfaces of n^- epitaxial layer 4, n-type diffusion layer 5 and p-type diffusion layer 6b, and p-type

diffusion layer 6a with an implantation dose, for example, of approximately 10^{15} ions/cm^2. P^+ diffusion layer 9 is formed by implantation of B or BF_2 to the surface of p-type diffusion layer 6a with an implantation dose, for example, of approximately 10^{15} ions/cm^2.

An interlayer insulating film 10 is formed on the main surface of semiconductor substrate 41 to cover the surface of semiconductor substrate 41. In interlayer insulating film 10, contact holes 11a-11c are formed. Interconnections 12a and 12b formed of polycrystalline silicon into which impurities are introduced (herein referred to as doped polysilicon) are formed on interlayer insulating film 10 to be connected electrically to respective regions discussed above via contact holes 11a-11c. Accordingly, p^+ diffusion layer 9 and n^+ diffusion layer 8a are electrically connected. Interconnection 12a (conductive layer) is electrically connected to signal input terminal 21 (Fig. 1) and device portion 25 (Fig. 1).

An operation of the surge protection circuit according to this embodiment is now described.

Referring to Figs. 1-3, when a surge voltage is applied to signal input terminal 21, the surge voltage is applied to n^+ diffusion layer 8b and a reverse voltage between the anode and cathode of diode 22 increases. Then, Zener breakdown of diode 22 occurs and a current flows from n^+ diffusion layer 8b to p-type diffusion layer 6b. From this p-type diffusion layer 6b, the current flows to p-type diffusion layer 6a which is the base region of npn transistor 23 to turn on npn transistor 23. Upon the turning-on of npn transistor 23, the current flows from n^- epitaxial layer 4 to n^+ diffusion layer 8a to release the surge voltage applied to signal input terminal 21 to interconnection 12a. In this way, application of the surge voltage to device portion 25 is prevented.

According to this embodiment, the cathode region of diode 22 is constituted of n^+ diffusion layer 8c, n^- epitaxial layer 4, n-type diffusion layer 5 and n^+ diffusion layer 8b. Of these layers, n^+ diffusion layer 8c electrically connected to interconnection 12b and n^+ diffusion layer 8b constituting the pn junction where Zener breakdown occurs are formed of different regions. Then, contact resistance relative to interconnection 12b

can be reduced by increasing the impurity concentration of n^+ diffusion layer 8c. Leakage of current can be prevented by decreasing respective impurity concentrations of p-type diffusion layer 6b and n^+ diffusion layer 8b. Further, as the pn junction between p-type diffusion layer 6b and n^+ diffusion layer 8b where Zener breakdown occurs is distant from field oxide film 7, a problem that the breakdown voltage of diode 22 increases can be solved. Here, the increase of the breakdown voltage is caused when electrons that are present in the depletion layer of the pn junction between the anode region and the cathode region are trapped in field oxide film 7 to expand the depletion layer of the pn junction. Accordingly, semiconductor device 51 having the surge protection circuit without suffering from current leakage and thus operating normally can be obtained.

The inventors of the present invention conducted the following experiment in order to confirm the above-discussed effect.

Specifically, current-voltage characteristics of a conventional semiconductor device having a surge protection circuit as well as current-voltage characteristics of the semiconductor device having the surge protection circuit according to this embodiment were examined. Referring to Figs. 4A and 4B, as for the current, a current flowing through npn transistor 23 (Fig. 1) is logarithmically plotted. The voltage is shown as a potential on signal input terminal 21 (Fig. 1) on the assumption that ground potential 24 (Fig. 1) is 0. V_1 indicates a breakdown voltage of diode 22 (Fig. 1).

It is seen from the experimental results that, a current flows in the conventional surge protection circuit even when the voltage is V_1 or less. This is due to current leakage of diode 22. On the other hand, according to the present invention, only a slight current on the order of 10^{-12} A flows when the voltage is V_1 or less. Then, when the voltage exceeds V_1, a large current suddenly flows. It is accordingly seen that no current leakage occurs in the semiconductor device having the surge protection circuit of the first embodiment of the present invention and thus a normal operation is performed.

Further, according to this embodiment, in surge protection circuit 31,

the cathode of diode 22 and the collector of transistor 23 are electrically connected to signal input terminal 21 and the anode of diode 22 and the base of transistor 23 are of the same conductivity type and connected electrically to each other.

The circuit is thus configured to ensure that diode 22 breaks down before transistor 23 does. Then, diode 22 breaks down to allow transistor 23 to be surely turned on, thereby allowing a surge voltage applied to signal input terminal 21 to be surely released. Therefore, surge protection circuit 31 capable of preventing a malfunction thereby operating normally can be implemented.

Moreover, according to this embodiment, n^+ diffusion layer 8b which is the cathode region constituting the pn junction where Zener breakdown occurs is formed to cover the upper surface of p-type diffusion layer 6b which is the anode region.

Then, such a configuration in which the pn junction where Zener breakdown occurs is distant from field oxide film 7 can readily be produced. Accordingly, an increase of the breakdown voltage of diode 22 can be prevented easily, the increase being caused when electrons in the depletion layer of the pn junction where Zener breakdown occurs are trapped in field oxide film 7 to cause an increased width of the depletion layer.

According to this embodiment, n^+ diffusion layer 8b which is the cathode region constituting the pn junction where Zener breakdown occurs is formed to cover the upper surface of p-type diffusion layer 6b which is the anode region. It is noted, however, that the present invention is not limited to such a configuration but applicable to a configuration in which the cathode region constituting the pn junction where Zener breakdown occurs is formed to cover the side of p-type diffusion layer 6b which is the anode region.

Second Embodiment

Referring to Figs. 5 and 6, according to this embodiment, an n^+ diffusion layer 13a is formed in n^- epitaxial layer 4 to enclose n^+ diffusion layer 8c. N^+ diffusion layer 13a is formed by implantation and diffusion of, for example, phosphorus glass into n^- epitaxial layer 4 so as to reach n^+

diffusion layer 2. Then, the collector region of npn transistor 23 is constituted of n^+ diffusion layer 8c, n^+ diffusion layer 13a, n^+ diffusion layer 2 and n^- epitaxial layer 4. N^+ diffusion layer 13a has its impurity concentration higher than that of n^- epitaxial layer 4.

It is noted that the configuration here is almost similar to that of the first embodiment shown in Figs. 1-3 except for the above-discussed details. The same components are thus denoted by the same reference character and description thereof is not repeated here.

In the semiconductor device having the surge protection circuit of this embodiment, the collector region of npn transistor 23 is constituted additionally of n^+ diffusion layer 13a. As the n^+ diffusion layer has a higher impurity concentration than that of the n^- epitaxial layer, the electrical resistance of the collector region (collector resistance) is low. The transistor can accordingly have an improved operating speed and the surge protection circuit can operate even when a surge of high frequency occurs as detailed below.

The operating speed of the transistor is higher as the transit time τ_B of minority carriers in the base region is shorter. Transit time τ_B of minority carriers in the base region is represented by the following formula:

$$\tau_B = \frac{Q_B}{I_C} \qquad (1)$$

where Q_B indicates charge of minority carriers implanted into the base region, I_C indicates collector current and τ_B indicates transit time of minority carriers in the base region. Referring to formula 1, transit time τ_B of minority carriers shortens with increase of collector current I_C. According to this embodiment, the n^+ diffusion layer is formed to decrease the collector resistance and accordingly increase collector current I_C. Consequently, transit time τ_B of minority carriers in the base region can be made shorter to improve the operating speed of the transistor, and the surge protection circuit can operate even when a surge of high frequency occurs.

Third Embodiment

Referring to Fig. 7, according to this embodiment, an n^+ diffusion

layer 13b is further formed in n^- epitaxial layer 4 on the right side (in Fig. 7) of p-type diffusion layer 6a. N^+ diffusion layer 13b is formed by a similar method to that for n^+ diffusion layer 13a. Then, the collector region of npn transistor 23 is constituted of n^+ diffusion layer 8c, n^+ diffusion layer 13a, n^+ diffusion layer 2, n^+ diffusion layer 13b and n^- epitaxial layer 4.

It is noted that the configuration here is almost similar to that of the second embodiment shown in Fig. 6 except for the above-discussed details. The same components are thus denoted by the same reference character and description thereof is not repeated here.

In the semiconductor device having the surge protection circuit of this embodiment, the collector region of npn transistor 23 is additionally constituted of n^+ diffusion layer 13b. As the n^+ diffusion layer has a higher impurity concentration than that of the n^- epitaxial layer, the collector resistance is low. In this way, the operating speed of the transistor can further be improved and the surge protection circuit can operate even when a surge of high frequency occurs.

Fourth Embodiment

Referring to Figs. 8 and 9, diode 22 is configured as discussed below according to this embodiment.

Specifically, in diode 22, the cathode region is constituted of n^+ diffusion layer 8c (first cathode region) formed in n^- epitaxial layer 4, n^- epitaxial layer 4 and n-type diffusion layer 5 (second cathode region) formed in n^- epitaxial layer 4. The anode region is constituted of p-type diffusion layer 6a formed in n^- epitaxial layer 4 and p^+ diffusion layer 9 formed in n-type diffusion layer 5 and p-type diffusion layer 6a. It is noted that p^+ diffusion layer 3b, p-type diffusion layer 6b and n^+ diffusion layer 8b are not formed.

According to this embodiment, a pn junction where Zener breakdown occurs is constituted of p^+ diffusion layer 9 and n-type diffusion layer 5. Here, p^+ diffusion layer 9 is formed to cover the upper surface of n-type diffusion layer 5. With semiconductor substrate 41 viewed from the above (Fig. 8), p^+ diffusion layer 9 is seen to have its periphery electrically connected to p-type diffusion layer 6a. Further, p-type diffusion layer 6a is

formed to enclose the side of n-type diffusion layer 5. The anode region constituted of p^+ diffusion layer 9 and p-type diffusion layer 6a is thus formed in the shape of a quadrangular prism and, in this quadrangular prism, n-type diffusion layer 5 serving as the cathode region is formed. Accordingly, the pn junction (pn junction formed of p^+ diffusion layer 9 and n-type diffusion layer 5) where Zener breakdown occurs is formed within the quadrangular prism, and is thus distant from field oxide film 7.

It is noted that the configuration here is almost similar to that of the first embodiment shown in Figs. 1-3 except for the above-discussed details. The same components are thus denoted by the same reference character and description thereof is not repeated here.

In the semiconductor device having the surge protection circuit of this embodiment, p^+ diffusion layer 9 which is the anode region constituting the pn junction where Zener breakdown occurs is formed to cover the upper surface of n-type diffusion layer 5 which is the cathode region.

Then, such a configuration in which the pn junction where Zener breakdown occurs is distant from field oxide film 7 can easily be produced. Accordingly, an increase of the breakdown voltage of diode 22 can be prevented easily, the increase being caused when electrons in the depletion layer of the pn junction where Zener breakdown occurs are trapped in field oxide film 7 to cause an increased width of the depletion layer.

According to this embodiment, p^+ diffusion layer 9 which is the anode region constituting the pn junction where Zener breakdown occurs is formed to cover the upper surface of n-type diffusion layer 5 which is the cathode region. It is noted, however, that the present invention is not limited to such a configuration but applicable to a configuration in which the anode region constituting the pn junction where Zener breakdown occurs is formed to cover the side of n-type diffusion layer 5 which is the cathode region.

Fifth Embodiment

Referring to Figs. 10 and 11, diode 22 is configured as described below according to this embodiment.

Specifically, in diode 22, the anode region is constituted of p^+ diffusion layer 3b formed in n^- epitaxial layer 4 and p-type diffusion layer 6a

formed in n^- epitaxial layer 4. The cathode region is constituted of n^+ diffusion layer 8c (first cathode region) formed in n^- epitaxial layer 4, n^- epitaxial layer 4 and n^+ diffusion layer 2 (second cathode region). P-type diffusion layer 6a is formed in n^- epitaxial layer 4 to extend and contact p^+ diffusion layer 3b. It is noted that n-type diffusion layer 5 and p-type diffusion layer 6b are not formed.

According to this embodiment, a pn junction where Zener breakdown occurs is constituted of p^+ diffusion layer 3b and n^+ diffusion layer 2. P^+ diffusion layer 3b and n^+ diffusion layer 2 are both formed within n^- epitaxial layer 4 (lower side in Fig. 11) and the pn junction where Zener breakdown occurs is distant from field oxide film 7.

It is noted that the configuration here is almost similar to that of the first embodiment shown in Figs. 1-3 except for the above-discussed details. The same components are thus denoted by the same reference character and description thereof is not repeated here.

According to this embodiment, the pn junction where Zener breakdown occurs is formed of p^+ diffusion layer 3b and n^+ diffusion layer 2 that are both regions of high impurity concentration respectively. P^+ diffusion layer 3b of the pn junction, however, locally has a lower impurity concentration for the following reason.

Specifically, p^+ diffusion layer 3b is formed by implantation of B into p^- substrate 1 with an implantation dose, for example, of approximately 10^{14} ions/cm^2 and heat treatment at a temperature, for example, of 1150°C. N^+ diffusion layer 2 is formed by implantation of Sb (antimony) into p^- substrate 1 with an implantation dose, for example, of approximately 10^{15} ions/cm^2 and heat treatment at a temperature, for example, of 1180°C. Here, as Sb has a lower diffusion coefficient than that of B, diffusion of Sb allows n^+ diffusion layer 2 to be formed near p^- substrate 1. On the other hand, as B has a higher diffusion coefficient than that of Sb, diffusion of B allows p^+ diffusion layer 3b to be formed in a region closer to the surface of substrate 41 relative to n^+ diffusion layer 2 (upper region in Fig. 11). In p^+ diffusion layer 3b thus produced, there is a difference in impurity concentration. In other words, in p^+ diffusion layer 3b, the region near the

surface of semiconductor substrate 41 (upper side in Fig. 11) locally has a high impurity concentration of B. On the other hand, in the pn junction with n^+ diffusion layer 2, p^+ diffusion layer 3b locally has a low impurity concentration of B and thus the depletion layer of the pn junction has an increased width. Then, the semiconductor device having the surge protection circuit without suffering from current leakage and operating normally can be obtained.

Further, according to this embodiment, p^+ diffusion layer 3b and n^+ diffusion layer 2 constituting the pn junction where Zener breakdown occurs are both formed in n^- epitaxial layer 4 formed in semiconductor substrate 41. Accordingly, the pn junction where Zener breakdown occurs is formed within semiconductor substrate 41 (on the lower side in Fig. 11) and heat generated in surge protection circuit 31 can efficiently be discharged to semiconductor substrate 41.

The first to fifth embodiments have been described in connection with the semiconductor device having the circuit in Fig. 1. The present invention, however, is not limited to this semiconductor device and applicable to any semiconductor device having a surge protection circuit connected electrically to a signal input terminal and having a diode and a transistor. As for the method of forming the impurity diffusion regions, the conditions are not limited to those of the embodiments and other conditions may be used.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.